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EXAMINER	
FLEURANTIN, JEAN B	

ART UNIT	PAPER NUMBER
2162	

NOTIFICATION DATE	DELIVERY MODE
01/03/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDOCKET@THOMPSONCOBURN.COM

Office Action Summary	Application No.	Applicant(s)	
	10/550,323	CHAMBERLAIN ET AL.	
	Examiner	Art Unit	
	JEAN B. FLEURANTIN	2162	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *40-52,54-64 and 98-175* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *51 and 52* is/are allowed.

6)☒ Claim(s) *40-43,46-50,54,59-64,98-125,128-137,139-161 and 163-175* is/are rejected.

7)☒ Claim(s) *44,45,55-58,126,127,138, and 162* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3).

Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :11/23/1020, 12/11/2010 and 06/22/2010.

DETAILED ACTION

1. This is in response to applicants arguments filed on 10/25/2010.

2. The following is the current status of claims:

Claims 1-39, 53, and 65-97 have been canceled.

Claims 105-175 have been added. The examiner discusses the newly added claims, set forth in sections 4, and 5.

Claims 40-52, 54-64, and 98-175 remain pending for examination.

Response to Arguments

3. Applicant's arguments, filed on 09/23/2010, with respect to claims have been fully considered but, have been found persuasive only to the extent the prior art of record does not specifically discloses the limitations "... re-configurable..." However, Villasenor discloses such limitations, set forth in sections 4, and 5.

However, applicant's arguments with respect to claims 44, 45, 55-58, 126, 127, 138, and 162 are persuasive, therefore, claims 44, 45, 55-58, 126, 127, 138, and 162 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, set forth in section 6.

It is noted, during patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification" Applicant always has the opportunity to amend the claims during prosecussion and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 162 USPQ 541,550-51 (CCPA 1969). The court found that applicant was advocating ... the impermissible importation of subject matter from the specification into the claim. See also In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997) (The court held that the PTO is not required, in the course of prosecution, to interpret claims in applications in the same manner as a court would interpret claims in an infringement suit. Rather, the "PTO applies to verbiage of the proposed claims the broadest reasonable meaning of

the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definition or otherwise that may be afforded by the written description contained in application's specification."). MPEP 2111.

The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. In re Cortright, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir.1999).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over USPT No. 4,464,718 issued to Dixon et al., ("Dixon") in view of "Configurable Computing Solutions For Automatic Target Recognition FPGAS for Custom Computing Machines" - Villasenor et al - 1996 ("Villasenor").

As per claim 40, Dixon discloses "a data processing system comprising:

"~~a data storage medium~~" [figure 1, item12];

"a processing device ~~in communication with the data storage medium~~" [i.e., cpu, main memory; figure 1, items 10, 12]; and

"a computer system having a system bus to control an operation of the processing device [i.e., bus system, figure 2, item 14], wherein the computer system is configured to communicate with the processing device over the system bus" [i.e., device connects via bus (22); col. 4, lines 38-40];

"wherein the processing device comprises a re-configurable ~~programmable~~ logic device configured to receive and process streaming the data, ~~as it passes between the data storage medium and~~

~~the computer system~~" [col. 4, lines 54-58], "through a ~~plurality of stages implemented on the programmable logic device as a processing~~ the pipeline comprising a plurality of pipelined data processing engines, the plurality of processing engines [figure 1, item 16], ~~each processing stage~~ being ~~dedicated~~ configured to [[a]] perform different processing operations, wherein the pipeline comprises a multi-functional pipeline" [col. 5, lines 47-51]; and "thereby define a function for the pipeline, the pipeline function being the combined functionality of each activated processing engines" [col. 6, lines 64-67]; and

"~~wherein the processing operations comprise at least two selected from the group consisting of a search operation, a data reduction operation, a data classification operation, an encryption operation, a decryption operation, a compression operation, and a decompression operation~~" [col. 6, lines 64-67, figure 4, items 18, 52].

Dixon fails to explicitly disclose through a pipeline deployed on the re-configurable logic device; the re-configurable logic device further comprises a control processor, wherein the control processor is configured to controllably activate or deactivate each processing engine in the pipeline. However, Villasenor discloses a pipeline deployed on the re-configurable logic device; the re-configurable logic device further comprises a control processor, wherein the control processor is configured to controllably activate or deactivate each processing engine in the pipeline [Villasenor page 70, col. 1, last Para to col. 2, first Para]. It would have been obvious to one ordinary skill in the art at the time the invention was made to modify the system/method of Dixon by a pipeline deployed on the re-configurable logic device; the re-configurable logic device further comprises a control processor, wherein the control processor is configured to controllably activate or deactivate each processing engine in the pipeline as disclosed by [Villasenor page 70, col. 2, section 1.1 overview of related work to page 71, col. 1, first Para]. Such a modification would allow the system/method of Dixon to provide reducing the configuration time linearly in accordance with the fraction of the gate array concerned [Villasenor page 71, col. 1, first Para], therefore, improving the reliability of the intelligent data storage and processing using fpga device.

As per claims 46, 59, and 101, Dixon discloses "the programmable logic device is an FPGA" [figure 1, and corresponding text].

As per claims 49, and 63, Dixon discloses "one of the at least two processing operations is a data reduction operation" [col. 8, lines 22-28].

As per claims 50, and 64, Dixon discloses "one of the at least two processing operations is a data classification operation" [col. 6, lines 63-78].

As per claim 54, the limitations of claim 54 are similar to claim 1, therefore, the limitations of claim 54 are rejected in the analysis of claim 1, and this claim is rejected on that basis.

As per claim 60, in addition to claim 40, Dixon further discloses "~~at least of~~ the processing engines comprises ~~operation of at least one stage is~~ a compression engine ~~operation~~" [col. 4, lines 32-35].

As per claims 98, and 99, Dixon discloses "the programmable logic device is further configured to deactivate a stage of the plurality of stages, whereby the deactivated stage acts as a pass through for the data it receives; the plurality of stages have an associated order, the order of the stages remaining the same whether any of the stages are deactivated" [col. 6, lines 61-68].

As per claim 100, in addition to claim 40, Dixon further discloses "wherein the processing device is configured to selectively activate and deactivate individual ones of the data processing stages to define a data processing pipeline, wherein a deactivated stage acts as a pass through for the data it receives [col. 8, lines 49-67], and wherein an activated stage performs the data processing operation to which that stage is dedicated upon the data it receives" [col. 6, lines 61-68; col. 10, lines 35-42].

As per claim 102, in addition to claim 40, Dixon further discloses "a hard disk drive accelerator for connection between a hard disk drive [figure 1, item 12] and a processor [figure 1, item 10], said accelerator comprising reconfigurable hardware logic arranged such that data read from the hard disk drive streams through the reconfigurable hardware logic prior to being passed on to the processor, wherein the reconfigurable hardware" [col. 4, lines 54-58].

As per claims 103, and 104, the limitations of claims 103, and 104 are similar to claims 98, and 99, therefore, the limitations of claims 103, and 104 are rejected in the analysis, and these claims are rejected on that basis.

As per claims 128-137, 139-141, 154-157, and 159-165, the limitations of claims 128-137, 139-141, 154-157, and 159-165 are similar to claims 40-42, therefore, the limitations of claims 128-137, 139-141, 154-157, and 159-165 are rejected in the analysis of claims 41-42, and these claims are rejected on that basis.

5. Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over USPT No. 4,464,718 issued to Dixon et al., ("Dixon") in view of "Configurable Computing Solutions For Automatic Target Recognition FPGAS for Custom Computing Machines" - Villasenor et al - 1996 ("Villasenor") as applied to claims above, and further in view of Background; page 1, line 1 to page 2, line 40, ("Background").

As per claim 105, in addition to claim 1, Dixon fails to explicitly disclose the streaming data comprises streaming financial information, the streaming financial information comprising data representative of a plurality of stocks and their associated prices, wherein the data reduction engine comprises a matching stage and a downstream summarization stage, wherein the matching stage is configured to search within the streaming financial information to find matching stocks of interest with respect to at least one data key. However, Background discloses the streaming data comprises streaming

financial information, the streaming financial information comprising data representative of a plurality of stocks and their associated prices, wherein the data reduction engine comprises a matching stage and a downstream summarization stage, wherein the matching stage is configured to search within the streaming financial information to find matching stocks of interest with respect to at least one data key [Background page 2, lines 12-14]. It would have been obvious to one ordinary skill in the art at the time the invention was made to modify the system of Dixon by streaming financial information, the streaming financial information comprising data representative of a plurality of stocks and their associated prices as disclosed by Background [Background page 7-14]. Such a modification would allow the system of Dixon to provide improve the reliability of the intelligent data storage and processing using FPGA devices.

As per claims 106-124, 142-153, 158, and 166-175, the limitations of claims 106-124, 142-153, 158, and 166-175 are similar to claim 105, therefore, the limitations of claims 106-124, 142-153, 158, and 166-175 are rejected in the analysis of claim 105, and these claims are rejected on that basis.

6. Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over USPT No. 4,464,718 issued to Dixon et al., ("Dixon") in view of "Configurable Computing Solutions For Automatic Target Recognition FPGAS for Custom Computing Machines" - Villasenor et al., 1996 ("Villasenor") as applied to claims above, and further in view of US Pub No. 2003/0163715 issued to Wong, ("Wong").

As per claims 41-42, 48, and 61, in addition to claim 1, Dixon fails to explicitly disclose receive ~~a continuous stream of~~ the encrypted data stream ~~from the data storage medium~~, (2) decrypt the received ~~continuous~~ encrypted data stream using the encryption engine to create a decrypted data stream, and (3) perform a search operation within the decrypted data stream using the search engine. However, Wong discloses receive ~~a continuous stream of~~ the encrypted data stream ~~from the data storage medium~~, (2) decrypt the received ~~continuous~~ encrypted data stream using the encryption engine to create a decrypted data stream, and (3) perform a search operation within the decrypted data stream using the search engine [Wong Para 0018, 0022, figures 2, 4]. It would have been obvious to one ordinary skill in the art at

the time the invention was made to modify the system of Dixon by decrypting the data stream as disclosed by Wong [Wong Para 0022]. Such a modification would allow the system of Dixon to provide significantly reduces development and manufacturing costs [Wong Para 0007, lines 10-12], therefore, improving the reliability of the intelligent data storage and processing using FPGA devices.

As per claims 43, and 47, in addition to claim 42, Dixon further discloses "the search operation is configured to determine whether a pattern match exists between a search key that is representative of data desired to be retrieved from the data storage medium" [i.e., comparison is continuously made between the count produced by the key address counter and the value stored in the key length register; col. 15, lines 4-9; col. 9, lines 17-26]. Dixon fails to explicitly disclose a data signal that is representative of the decrypted data stream. However, Wong discloses a data signal that is representative of the decrypted data stream [Wong Para 0018, 0022, figures 2, 4]. Such a modification would allow the system of Dixon to provide significantly reduces development and manufacturing costs [Wong Para 0007, lines 10-12], therefore, improving the reliability of the intelligent data storage and processing using FPGA devices.

Allowable Subject Matter

7. Claims 44, 45, 55-58, 126, 127, 138, and 162 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 51, and 52 are allowed.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

CONTACT INFORMATION

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEAN B. FLEURANTIN whose telephone number is (571)272-4035. The examiner can normally be reached on 10:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JOHN E. BREENE can be reached on 571 - 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jean B. Fleurantin/
Primary Examiner, Art Unit 2162